

## REMARKS/ARGUMENTS

### 1. Interview Summary

The arguments and amendments presented herein include the arguments and amendments Applicants discussed with the Examiner during phone interview held on August 20, 2007. Applicants submit that the arguments presented herein make the substance of the phone interview of record to comply with 37 CFR 1.133.

During the phone interview, the Examiner requested applicants to submit the arguments Applicants presented in the Interview Request Form, a copy of which is submitted herewith, distinguishing claims from the cited art. The Examiner said that the claims likely distinguish over the cited art based on the arguments presented in the Interview Request Form, which are further presented herein. The Examiner further said he would update his search. If the Examiner believes that further information on the interview needs to be made of record to comply with the requirements, Applicants request the Examiner to identify such further information.

### 2. Information Disclosure Statement Not Reviewed

On August 24, 2006, Applicants submitted an Information Disclosure Statement (“IDS”). In the Office Action, the Examiner did not indicate that he reviewed the reference cited in this IDS. Applicants request that the Examiner review and indicate the reference cited in the August 24, 2006 IDS as reviewed.

### 3. Claim Amendments and Objections

Applicants amended claim 1 to remove extra period at end; amended claims 9 and 21 to add the word “claim” before the claim number; amended claim 23 to change the dependency to claim 13; and amended claim 24 to remove the limitation reference numerals.

The Examiner objected to claims 27-38 for the “article of manufacture” language and requested the use of “computer readable storage medium” language. Applicants amended claim 27 to recite that the “article of manufacture” comprises “at least one of a hardware device having hardware logic and a computer readable storage medium having code”. Applicants submit that these added requirements are disclosed on at least para. [0011] on pg. 4 and para. [0018] on pg. 7

of the Specification. Applicants submit that this amendment to claim 27 overcomes the grounds of the Examiner's objection.

4. Allowable Subject Matter

The Examiner found that claims 7, 11, 19, 23, 26, 33, and 37 would be allowed if written in independent form. (Office Action, pg. 4) Applicants submit that these claims are patentable over the cited art in their current form because they depend from base claims which are patentable over the cited art for the reasons discussed below.

5. Claims 1-6, 8-10, 12-18, 20-22, 24, 25, 27-32, 34-36, and 38 are Patentable Over the Cited Art

The Examiner rejected claims 1-6, 8-10, 12-18, 20-22, 24, 25, 27-32, 34-36, and 38 as anticipated (35 U.S.C. §102) by Kim (U.S. Patent No. 5,446,738). Applicants traverse for the following reasons.

Claims 1, 13, 24, and 27 concern constructing a packet and require: receiving a request to construct one packet, including information on at least one header and a payload to include in the packet; generating the at least one header for the received request; writing the generated at least one header in a first queue; requesting the payload to include in the packet; writing the received payload to a second queue; reading the generated at least one header and payload from the first and second queues; and including the read at least one header and payload in the packet.

The Examiner cited FIG. 6A with respect to the claim requirements of reading the generated at least one header and payload from the first and second queues and including the read at least one header and payload in the packet. (Office Action, pg. 3) Applicants traverse.

FIG. 6a shows a priority encoder controlling the reading of cells from the input stage from ATM cell input circuits a. (col. 8, lines 5-12) A header select signal circuit d2 generates header select signals to read headers from the ATM cell input circuits and generate a header input start signal, a header write clock signal and an input port number to apply the read headers to the link table processing circuit. (col. 8, lines 12-20) Nowhere does this cited discussion of FIG. 6a anywhere disclose reading header and payload from separate queues and then including the read payload and header from different queues in a packet.

The Examiner has not cited any part of Kim that discloses that FIG. 6a concerns reading separate payload and header from separate queues to construct a packet. Instead, the cited discussion of Kim with respect to FIG. 6a discusses processing headers to apply to a link table processing circuit.

The Examiner further cited FIG. 3A and col. 6, lines 51-62 of Kim with respect to the claim limitations (Office Action, pg. 2)

The cited col. 6 discusses a header buffer a3 to receive header data from write control logic in response to a header write signal and a payload buffer a2 to receive payload data from the write control logic. The payloads are sent over a bus in response to a payload transmission select signal. (col. 7, lines 43-57).

Applicants submit that the cited sections of Kim do not disclose the claim requirements of reading header and payload from separate queues and then including the read payload and header from different queues in a packet.

Accordingly, claims 1, 13, 24, and 27 are patentable over the cited art because the requirements of these claims are not disclosed in the cited Kim.

Claims 2-6, 8-10, 12, 14-18, 20-22, 25, 28-32, 34-36, and 38 are patentable over the cited art because they depend from one of claims 1, 13, 24, and 27, which are patentable over the cited art for the reasons discussed below. Moreover, the following claims provide further grounds of patentability over the cited art.

Claims 3, 15, and 29 depend from claims 1, 13, and 27, respectively, and additionally require signaling header complete in response to writing one header to the first queue and signaling payload complete in response to writing the payload to the second queue.

The Examiner cited col. 8, lines 1-4 of Kim as disclosing the additional requirements of these claims. (Office Action, pg. 3) Applicants traverse for the following reasons.

The cited col. 8 mentions that an ATM multiplexer select signal and a data reception complete signal generation circuit c2 for receiving the ATM multiplexer select signal and generating a data reception complete signal indicative of the reception of the transmission data.

Although the cited col. 8 mentions generating a complete signal indicating reception of transmission of data, nowhere does the cited col. 8 disclose or mention the claim requirements of signaling header complete in response to writing one header to the first queue and signaling payload complete in response to writing the payload to the second queue. In other words, the

Examiner has not cited any part of Kim that mentions signaling complete in response to writing to the payload buffer a2 and header buffer a3.

Accordingly, claims 3, 15, and 29 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclose in the cited Kim.

Claims 4, 16, and 30 depend from claims 3, 15, and 29, respectively, and further require that the at least one header and payload are included in the packet in response to receiving signals that all headers for the packet to construct are written to the first queue and the payload for the packet to construct is written to the second queue.

The Examiner cited FIG. 2 of Kim as disclosing the additional requirements of these claims. (Office Action, pg. 3) The cited FIG. 2 shows a block diagram of an ATM multiplexing system with ATM cell input circuits. In response to a cell reception start request signal, each ATM cell input circuit separates a header and payload from the cell stream. A priority encoder d reads the received headers and sends the resultant header changing and link service priority information to a link table e. The link table processing circuit e sends changed headers and service priority information to an ATM cell output circuit f. The ATM cell output circuit f designates a payload output port for the cell transmission based on order and performs header transmission corresponding to payload to be transmitted, before the payload transmission. (Kim, col. 5, line 41 to col. 6, line 28).

Although the cited FIG. 2 provides components to process payload and headers, the Examiner has not cited any part of Kim that discloses or mentions the particular claim requirement that at least one header and payload are included in the packet in response to receiving signals that all headers for the packet to construct are written to the first queue and the payload for the packet to construct is written to the second queue. There is no mention in the cited Kim that packets of headers and payloads from the first and second queue are constructed in response to all headers for the packet written to the first queue and the payload to the second queue.

Accordingly, claims 4, 16, and 30 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclose in the cited Kim.

Claims 5, 17, and 31 depend from claims 4, 16, and 30, respectively, and further require that writing the header and signaling header complete are performed by a header engine, wherein writing the received payload and signaling payload complete are performed by a payload engine,

and wherein including the read at least one header and payload in the packet are performed by a completion engine in response to receiving the signals.

The Examiner cited col. 8, lines 1-4 of Kim as disclosing the claim requirement that a completion engine includes the read at least one header and payload in the packet in response to receiving the signals. (Office Action, pg. 3) Applicants traverse.

The cited col. 8 mentions that an ATM multiplexer select signal and a data reception complete signal generation circuit c2 for receiving the ATM multiplexer select signal and generating a data reception complete signal indicative of the reception of the transmission data.

Although the cited col. 8 mentions generating a complete signal indicating reception of transmission of data, this cited col. 8 does not disclose or mention the claim requirement of a completion engine that includes the read at least one header and payload in the packet in response to receiving the signals.

Accordingly, claims 5, 17, and 31 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Kim.

Claims 8, 20, and 34 depend from claims 1, 13, and 27 and further require accessing the payload from a system memory in response to receiving the request, wherein the accessed payload is written to the second queue.

The Examiner cited the above discussed FIG. 3A, FIG. 6A, and cols. 6, lines 51-62 with respect to claims 8, 20, and 34. (Office Action, pgs. 2-3) However, the Examiner did not mention which particular section of Kim discloses that the payload is accessed from a system memory.

Moreover, the cited Kim discusses how to process a payload within various circuits, such as ATM cell input circuits as shown in FIG. 3A (col. 6, lines 38-43) and a priority encoder d (col. 8, lines 5-10). Although the cited Kim discusses processing payloads in buffers in a circuit, nowhere does this cited Kim disclose that the payload placed in the queue is accessed from a system memory as claimed.

Accordingly, claims 8, 20, and 34 provide additional grounds of patentability over the cited art because the additional requirements of these claims are not disclosed in the cited Kim.

Amdt. dated September 14, 2007  
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Conclusion

For all the above reasons, Applicant submits that the pending claims 1-38 are patentable. Should any additional fees be required beyond those paid, please charge Deposit Account No. 50-0585.

The attorney of record invites the Examiner to contact him at (310) 553-7977 if the Examiner believes such contact would advance the prosecution of the case.

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